Amendments of the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the above-identified application.

Listing of Claims:

1. (currently amended) Circuitry operative in two modes for providing a dynamically adjustable bandwidth comprising:

a phase frequency detector receiving as input a clock signal and having a signal output;

a phase detector receiving as input a clock data recovery (CDR) signal and having a signal output;

a charge pump having a pump input coupled to the signal output of the phase frequency detector during a first of the two modes, and coupled to the signal output of the phase detector during a second of the two modes, and having a pump output;

a loop filter having a filter input coupled to the pump output of the charge pump and having a filter output;

a voltage controlled oscillator having an oscillator input coupled to the filter output of the loop filter and having an oscillator output;

a divider circuit having a divider input coupled to the oscillator output of the voltage controlled oscillator and having a divider output that feeds back to the input of the phase frequency detector; and

control circuitry that receives as input at least one control signal and is operative to dynamically adjust a setting in at least one of the charge pump, the loop

filter, the voltage controlled oscillator, and the divider circuit while the circuitry is processing data.

2. (currently amended) The circuitry of claim 1 wherein the circuitry operates as a [[is]] clock data recovery circuitry during the first mode and as a phase locked loop circuitry in the second mode.

3. (canceled)

4. (original) The circuitry of claim 1 wherein the setting in the charge pump that can be dynamically adjusted is current.

5. (original) The circuitry of claim 1 wherein the setting in the loop filter that can be dynamically adjusted is at least one of a resistor value and a capacitor value.

6. (original) The circuitry of claim 1 wherein the setting in the voltage controlled oscillator that can be dynamically adjusted is a voltage gain.

7. (original) The circuitry of claim 1 wherein the setting in the divider circuit that can be dynamically adjusted is a scale factor.

8. (original) The circuitry of claim 1 wherein the at least one control signal includes a value for the setting.

9. (original) The circuitry of claim 1 wherein the at least one control signal is indicative of whether a value of the setting is to be increased or decreased.

10. (original) The circuitry of claim 1 wherein the at least one control signal includes at least one data bit that corresponds to information on a value for the setting stored in a lookup table in the control circuitry.

11. (original) The circuitry of claim 1 wherein the at least one control signal is set by a programmable logic device.

12. (original) The circuitry of claim 1 wherein the at least one control signal is set by circuitry external to a programmable logic device.

13. (original) The circuitry of claim 1 wherein the at least one control signal is set by user input.

14. (original) A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

circuitry as defined in claim 1 coupled to the processing circuitry and the memory.

15. (original) A printed circuit board on which is mounted the apparatus as defined in claim 1.

16. (original) The printed circuit board defined in claim 15 further comprising:

a memory mounted on the printed circuit board and coupled to the circuitry.

17. (original) The printed circuit board defined in claim 15 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the apparatus.

18. (currently amended) A programmable logic device comprising:

clock data recovery (CDR) circuitry selectively operative in two modes that receives as input a reference clock signal and a CDR signal and in a first selected mode of the two modes is operative to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal, and in a second selected mode of the two modes is operative to use the recovered clock signal to recover clock information and data information from the CDR signal; and

control circuitry that receives as input at least one control signal and is operative to dynamically adjust a bandwidth of the CDR circuitry by changing a setting in at least one component in the CDR circuitry while the CDR circuitry is processing data, wherein the control circuitry is capable of changing the setting in a charge pump, a loop filter, a voltage controlled oscillator, and a divider circuit in the CDR circuitry.

19. (currently amended) The programmable logic device of claim 18 wherein the CDR circuitry comprises:

a phase frequency detector receiving as input the reference clock signal and having a signal output;

a phase detector receiving as input a CDR signal and having a signal output;

the charge pump having a pump input coupled to the signal output of the phase frequency detector during the first mode, and coupled to the signal output of the phase detector during the second mode, and having a pump output;

the loop filter having a filter input coupled to the pump output of the charge pump and having a filter output;

the voltage controlled oscillator having an oscillator input coupled to the filter output of the loop filter and having an oscillator output; and

the divider circuit having a divider input coupled to the oscillator output of the voltage controlled oscillator and having a divider output that feeds back to the input of the phase frequency detector.

20. (canceled)

21. (Original) The programmable logic device of claim 19 wherein the setting in the at least one component comprises current in the charge pump.

22. (original) The programmable logic device of claim 19 wherein the setting in the at least one component comprises a resistor value in the loop filter.

23. (original) The programmable logic device of claim 19 wherein the setting in the at least one component comprises a capacitor value in the loop filter.

24. (original) The programmable logic device of claim 19 wherein the setting in the at least one component comprises a voltage gain in the voltage controlled oscillator.

25. (original) The programmable logic device of claim 19 wherein the setting in the at least one component comprises a scale factor in the divider circuit.

26. (original) The programmable logic device of claim 18 wherein the at least one control signal is set by the programmable logic device.

27. (original) The programmable logic device of claim 18 wherein the at least one control signal is set by circuitry external to the programmable logic device.

28. (original) The programmable logic device of claim 18 wherein the at least one control signal is set by user input.

29. (currently amended) A programmable logic device comprising:

phase locked loop (PLL) circuitry selectively operative in two modes that receives as input a clock signal and in a first selected mode of the two modes is operative to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the clock signal, and in a second selected mode of the two modes is operative to drive another component external to the PLL circuitry in the programmable logic device with the recovered clock signal; and

control circuitry that receives as input at least one control signal and is operative to dynamically adjust a bandwidth of the PLL circuitry by changing a setting in at least one component in the PLL circuitry while the PLL circuitry is processing data, wherein the control circuitry is

capable of changing the setting in a charge pump, a loop filter, a voltage controlled oscillator, and a divider circuit in the PLL circuitry.

30. (currently amended) The programmable logic device of claim 29 wherein the PLL circuitry comprises:

a phase frequency detector receiving as input the reference clock signal and having a signal output;

a phase detector receiving as input a clock data recovery (CDR) signal and having a signal output;

the charge pump having a pump input coupled to the signal output of the phase frequency detector during the first mode, and coupled to the signal output of the phase detector during the second mode, and having a pump output;

the loop filter having a filter input coupled to the pump output of the charge pump and having a filter output;

the voltage controlled oscillator having an oscillator input coupled to the filter output of the loop filter and having an oscillator output; and

the divider circuit having a divider input coupled to the oscillator output of the voltage controlled oscillator and having a divider output that feeds back to the input of the phase frequency detector.

31. (canceled)

32. (original) The programmable logic device of claim 30 wherein the setting in the at least one component comprises current in the charge pump.

33. (original) The programmable logic device of claim 30 wherein the setting in the at least one component comprises a resistor value in the loop filter.

34. (original) The programmable logic device of claim 30 wherein the setting in the at least one component comprises a capacitor value in the loop filter.

35. (original) The programmable logic device of claim 30 wherein the setting in the at least one component comprises a voltage gain in the voltage controlled oscillator.

36. (original) The programmable logic device of claim 30 wherein the setting in the at least one component comprises a scale factor in the divider circuit.

37. (original) The programmable logic device of claim 29 wherein the at least one control signal is set by the programmable logic device.

38. (original) The programmable logic device of claim 29 wherein the at least one control signal is set by circuitry external to the programmable logic device.

39. (original) The programmable logic device of claim 29 wherein the at least one control signal is set by user input.

40. (new) The circuitry of claim 1 further comprising:

CDR control circuitry operative to provide a control signal to the charge pump, wherein the control signal is operative to select between the first and second modes.

41. (new) The circuitry of claim 40 wherein the control signal selects the first mode in response to an indication that the clock signal has a phase and frequency which respectively corresponds to a phase and frequency of the oscillator output.

42. (new) The circuitry of claim 19 further comprising:

CDR control circuitry operative to provide a control signal to the charge pump, wherein the control signal is operative to select between the first and second modes.

43. (new) The circuitry of claim 42 wherein the control signal selects the first mode in response to an indication that the clock signal has a phase and frequency which respectively corresponds to a phase and frequency of the oscillator output.

44. (new) The programmable logic device of claim 29 wherein the external component in the programmable logic device comprises CDR circuitry.

45. (new) The circuitry of claim 30 further comprising:

CDR control circuitry operative to provide a control signal to the charge pump, wherein the control signal is operative to select between the first and second modes.

46. (new) The circuitry of claim 45 wherein the control signal selects the first mode in response to an indication that the clock signal has a phase and frequency which respectively corresponds to a phase and frequency of the oscillator output.